AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to (i) couple to a first legacy USB peripheral device and (ii) communicate to said first legacy USB peripheral device as a host ~~through a first~~ interface;

a second circuit coupled to said first circuit and configured to communicate ~~through a second~~ as an OTG host/peripheral interface ~~as a host when in a first mode and as a peripheral when in a second mode~~; and

a third circuit configured to generate one or more control signals configured to (i) control operation of said first and said second circuits and (ii) transfer information between said first and said second circuits, wherein said first legacy USB peripheral device appears to be a USB on-the-go (OTG) dual role device (DRD).

2. (CURRENTLY AMENDED) The apparatus according to claim 1, further comprising a first device coupled to said first ~~interface~~ circuit.

3. (CURRENTLY AMENDED) The apparatus according to claim 2, wherein said first device comprises ~~a~~ said first legacy USB peripheral device.

4. (CURRENTLY AMENDED) The apparatus according to claim 2, further comprising a second device coupled to said second ~~interface~~ circuit.

5. (ORIGINAL) The apparatus according to claim 4, wherein said second device comprises a USB OTG dual role device (DRD).

6. (CURRENTLY AMENDED) The apparatus according to claim 4, wherein said second device comprises a second legacy USB device.

7. (ORIGINAL) The apparatus according to claim 1, wherein said first circuit comprises a USB controller.

8. (ORIGINAL) The apparatus according to claim 1, wherein said second circuit comprises a USB 2.0 on-the-go (OTG) dual role device (DRD) controller.

9. (ORIGINAL) The apparatus according to claim 1, wherein said third circuit comprises a device selected from the group consisting of a microcontroller, a microprocessor, an ASIC, a DSP, and a PLD.

10. (ORIGINAL) The apparatus according to claim 1, wherein said third circuit is configured in response to one or more computer executable instruction.

11. (ORIGINAL) The apparatus according to claim 10, wherein said computer readable instructions comprise firmware.

12. (ORIGINAL) The apparatus according to claim 10, wherein said computer readable instructions comprise software.

13. (ORIGINAL) The apparatus according to claim 2, wherein said apparatus is integrated with said first device.

14. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured as a stand alone accessory.

15. (ORIGINAL) The apparatus according to claim 2, wherein said apparatus is configured to add USB OTG dual role device (DRD) capabilities to said first device with no modifications to said first device.

16. (CURRENTLY AMENDED) An apparatus comprising:

means for communicating as a host interface with a legacy USB peripheral device; and

means for communicating as a USB OTG dual role device (DRD) coupled to said means for communicating as a host interface; and

means for ~~controlling~~ generating one or more control signals configured (i) to control said means for communicating as a host interface and said means for communicating as a USB OTG dual

role device and ~~transferring~~ (ii) to communicate information between said means for communicating as a host interface with ~~a~~ said legacy USB peripheral device and said means for communicating as a USB OTG dual role device (DRD), wherein said legacy USB peripheral device appears to be a USB on-the-go (OTG) dual role device (DRD).

17. (PREVIOUSLY PRESENTED) A method for adding USB on-the-go (OTG) dual role device (DRD) capability to a legacy USB peripheral device comprising the steps of:

configuring a host interface to couple to said legacy USB peripheral device;

coupling an OTG host/peripheral interface to said host interface; and

generating one or more control signals configured (i) to control operation of said host interface and said OTG host/peripheral interface and (ii) to communicate information between said host and said OTG host/peripheral interfaces, wherein said legacy USB peripheral device appears to be a USB on-the-go (OTG) dual role device (DRD).

18. (ORIGINAL) The method according to claim 17, further comprising the steps of:

enumerating a first device; and

responding to an enumeration request from a second device with descriptors received from said first device modified to indicate OTG DRD capability.

19. (ORIGINAL) The method according to claim 17, further comprising the steps of:

responding to an IN token received through said OTG host/peripheral interface with a NAK;

sending an IN token via said host interface;

repeatedly responding with NAKs to IN tokens from said OTG host/peripheral interface until data is received via said host interface; and

sending said data received from said host interface via said OTG host/peripheral interface in response to an IN token.

20. (ORIGINAL) The method according to claim 17, further comprising the steps of:

polling said host interface for an OUT token;

polling said OTG host/peripheral interface for an OUT token;

sending data received from either interface to the other interface.

21. (ORIGINAL) A computer readable media comprising computer executable instructions for performing the steps according to claim 17.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first circuit, said second circuit and said third circuit are implemented in a single integrated circuit (IC).

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein:

said first circuit comprises (i) a host controller configured to operate in response to one or more first control signals and (ii) a first analog block configured to detect or control one or more operations selected from the group consisting of VBUS pulsing, ID pin sensing, overcurrent control and detection, host/slave LED indication, and VBUS On/Off control;

said second circuit comprises (i) a host/peripheral controller configured to operate in response to one or more second control signals and (ii) a second analog block configured to detect or control one or more operations selected from the group consisting of VBUS pulsing, ID pin sensing, overcurrent control and detection, host/slave LED indication, and VBUS On/Off control; and

said third circuit is further configured to generate said one or more first control signals and said one or more second control signals.